To: Glenn Unger
From: Dave Sheppard
Date: 9-27-02
Re: Results of GARC V1 Testing

Summary:

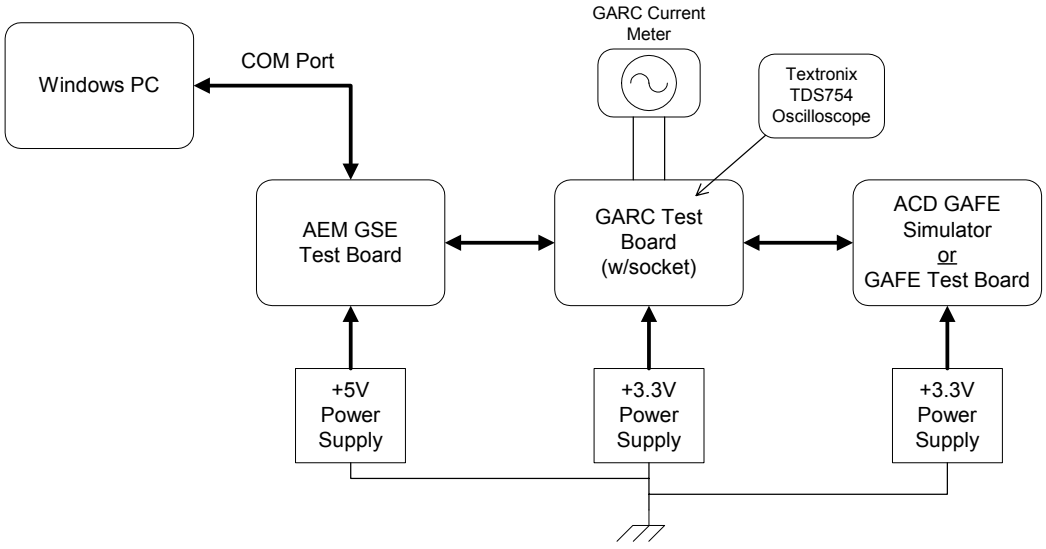
On 9-6-02, we received 10 GARC Version 1 ASICs (T25S – AL GARC1 64588). These were serialized with numbers 1 – 10 and tested using the GARC GSE test board at GSFC (room 62 lab). This report summarizes the results of the testing that was done.

It was found that the fabrication was successful and that there was complete functionality in the seven of ten GARC ASICs tested (we intend to test the remaining three ASICs, too). GARC V1 was also tested with a modified GAFE V2 and this interface was verified. The GARC V1 ASIC performed similarly to the GARC test board that has used as the logic testbench.

Deviations from expected values were found in the GARC LVDS driver currents. Consultation with SLAC indicated that this was likely due to a layout feature that may be easily corrected in GARC V2. It will be desirable to submit a second version of the GARC which incorporates updates to both the logic and layout.

Test Setup:

The following test setup was utilized to test GARC V1 in building 2, room 62.



Data was recorded in the as-run copy of the GARC V1 Design Description and test plan, as well as in notebooks (Sheppard) #3 (pages 113 – 151) and #4 (pages 1 – 19).

Details of the Test:

The test was performed using the 8/15/02 GARC V1 Design Description and Test Plan as a guide. The software used to run the AEM GSE test board is a series of DOS-based C programs that originated with Bob Baker. During this test, we specifically used the following code:

aem3.exe The basic GSE used for sending commands, reading back registers, sending ACD triggers, and capturing event data.

aem4.exe Automated routine to test all the GAFE registers.

aem5.exe Automated routine to test all the GARC registers.

aem7.exe Automated routine to read back all the register defaults after reset.

aem9.exe Used for sending a GAFE strobe and an ACD trigger separated by about 1 μsec for self-trigger testing.

Referencing each section of the GARC V1 Test Plan, the following tests were performed:

Test Plan Section	Test Name	Result
5.0	Initial Reset Test	All values properly initialized and read back during this section.
6.0 (6.1 – 6.3)	GARC Power Measurements	GARC power was measured at +3.0V, +3.3V, and +3.6V. The current measured was lower than expected due to bias voltage drops in the LVDS circuitry.
6.4	GARC Bias Resistor voltages	These voltages were measured in more detail than originally planned. A summary of these results is included below in Appendix 1.
7.0 (7.1 –7.33)	GARC Register Read/Write Tests	All GARC registers passed automated testing via aem5.c → 'h0000, 'hAAAA, 'h5555, 'hFFFF
8.0	GARC Test Pin Mux Verification	Verified to switch correctly via GARC_Mode[10] command.
9.0	Hold Delay Operation	Functions as designed.
10.0	AEM VETO Signal Functionality	Veto_Delay, Veto_Width, Veto Enable/Disable, Minimum input width, input extended width, and input double pulse test all work as designed. All VETO outputs were checked.
11.0	HitMap Functionality	Width test, Delay test, Deadtime stretch test, Minimum width test, and extended pulse test all work as designed.
12.0	Synchronization of HitMap Latch to the Input	Verified.

	Discriminator	
13.0	Strobe Test	GAFE Strobe Verified.
14.0	Test of MAX5121 DAC Control	Digital input, analog output, and digital readback all verified.
15.0	MAX145 ADC control test	Verified.
16.0	ADC Commandable Acquisition Time Test	Verified.
17.0	GARC Return Data Parity test	Verified via oscilloscope. Modification to procedure here since GSE isn't yet setup for this test.
18.0	Triple Modular Redundancy circuit test	Verified. Note that in the procedure there is an error on the last line of the table on page 44.
19.0	Look-At-Me command test	Verified.
20.0	GAFE Parity Command test	Verified with modified GAFE V2.
21.0	LVDS Driver Current test	This test was performed and the results did not pass comparison to the ICD specification (although the margin is sufficient that the digital signals still work). More on this below in Appendix 1.
22.0	FREE Board ID Circuit	Verified.
23.0	Maximum PHA Test	Verified.
24.0	PHA Enable/Disable Test	OK. This works as in the ICD, but probably should be changed for Version 2. More on this below.
25.0	PHA Threshold Verification Test	Verified.
26.0	GARC Diagnostics test	Verified.
27.0	GAFE Interface test.	Verified with modified GAFE V2 (modified to send GAFE_RTND)
28.0	GAFE Logic Test	Verified with modified GAFE V2

Issues to Address:

(1) Differences in LVDS driver currents. The LVDS drive current is determined by the $V_{G\text{-}S}$ of a PMOS transistor in each cell. The source voltage is apparently dropping as the distance from pin 24 (DVDD) increases. In version 2, the suggested fix is to put a wide track of metal3 in parallel to the existing track to decrease this impedance. The data that was taken during the exploration of this situation is included in Appendix 1.

(2) Measurements of ACD_CLK, NSCMD, and NSDATA Phasing. We investigated the phasing of the input clock vs. input commands and the input clock vs. output NSDATA. The clock and command data appear to work correctly. The NSDATA also works correctly but is susceptible to delays

introduced by cabling. These measurements are detailed in a document produced by Bob Baker, a copy of which is included in Appendix 2. As a result of these measurements, we propose that we add a 12^{th} bit to the GARC_Mode register to enable the NSDATA to be commanded to be clocked out on either the positive or negative edge of the ACD_CLK. This should ensure that the NSDATA as received at the AEM will not transition near the latching edge of the clock at the AEM.

At the GARC pins, the delay from the posedge of the ACD_CLK to the data transition time is measured at 23 nsec.

Updates Proposed for GARC V2:

(1) Add additional metal3 in the layout to provide a lower impedance for LVDS driver currents distribution.

(2) GARC_VERSION will be updated from 1 to 2.

(3) The HLD_Enable registers HLD_EN0 and HLD_EN1 are redundant and will be eliminated.

(4) The GAFE_RESET_DURATION will be increased to 12.8 μsec from ~ 100 nsec. This did not cause a problem in testing, but we have decided a longer reset would ensure a better design.

(5) The internal GARC_Reset command will now use a digital one-shot to preclude a race-condition found in the V1 logic (this V1 reset was measured at 82 nsec). The GARC V2 reset will now be 300 nsec.

(6) Update the ZS_MAP to show as active only bits that are above the PHA threshold, enabled, and to be sent. Presently, the PHA_enable bits are only effective in the zero-suppressed mode. We will change this to be effective in both trigger modes. Changes to the AEM-ACD ICD will have to be made to reflect this change.

(7) All reset circuits will now be deglitched. In GARC V1, the power on reset circuit is not deglitched.

(8) In GARC V1 the GAFE receives clocks during the reset time. These are unnecessary and will be eliminated.

(9) A command to implement a phase shift (e.g., 180 degrees) on the returned NSDATA will be included via the GARC_Mode command.

Appendix 1: Data from GARC V1 Biasing Tests, 9/16/02

Several GARC V1 ASICs were tested 9/6/02 – 9/13/02 and the following response to bias current variations was recorded. Preliminary measurements indicate minimal variation from ASIC to ASIC.

The GARC Test Board was utilized for GARC V1 testing. The GARC uses the following bias resistors:

R19 HLD_WOR_BIAS (HLD wired-or biasing)
R16 BIAS_RCVR (LVDS receiver biasing)
R15 BIAS_DRV_H (ACD-AEM driver biasing)
R16 BIAS_DRV_L (GARC-GAFE driver biasing)
R20 LVDS_PRESET_ADJ (driver servo-voltage adjust)

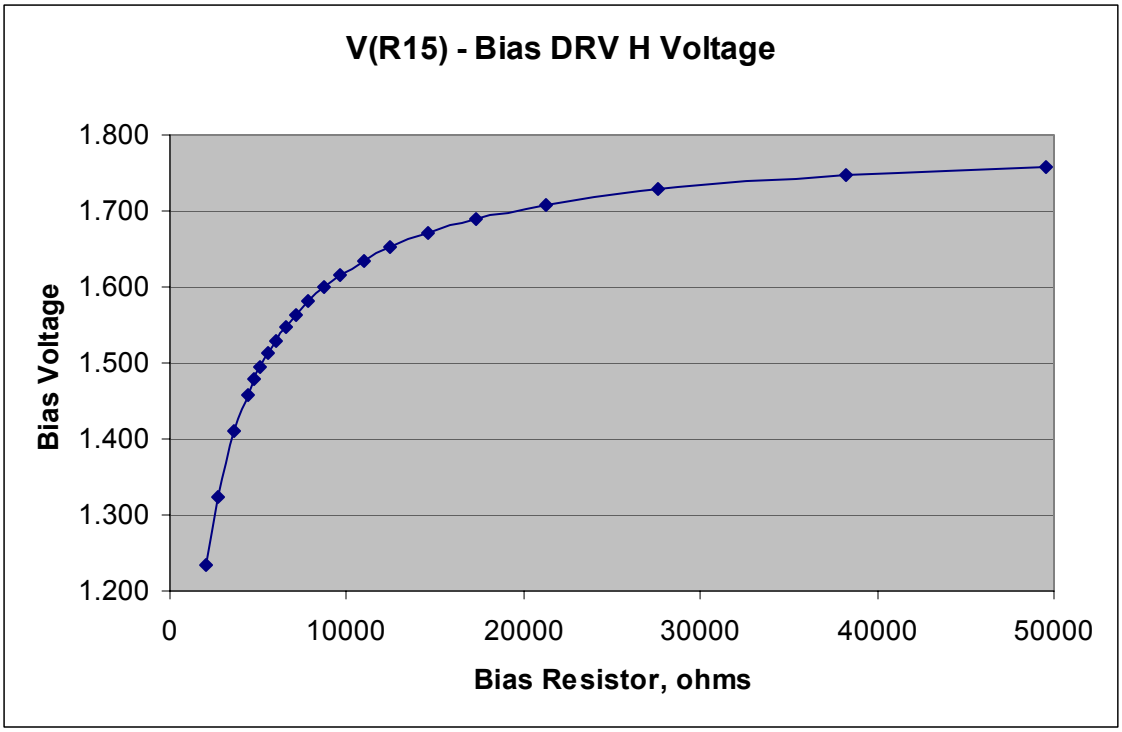
The following currents were measured on GARC V1 with the biases adjusted as shown below:

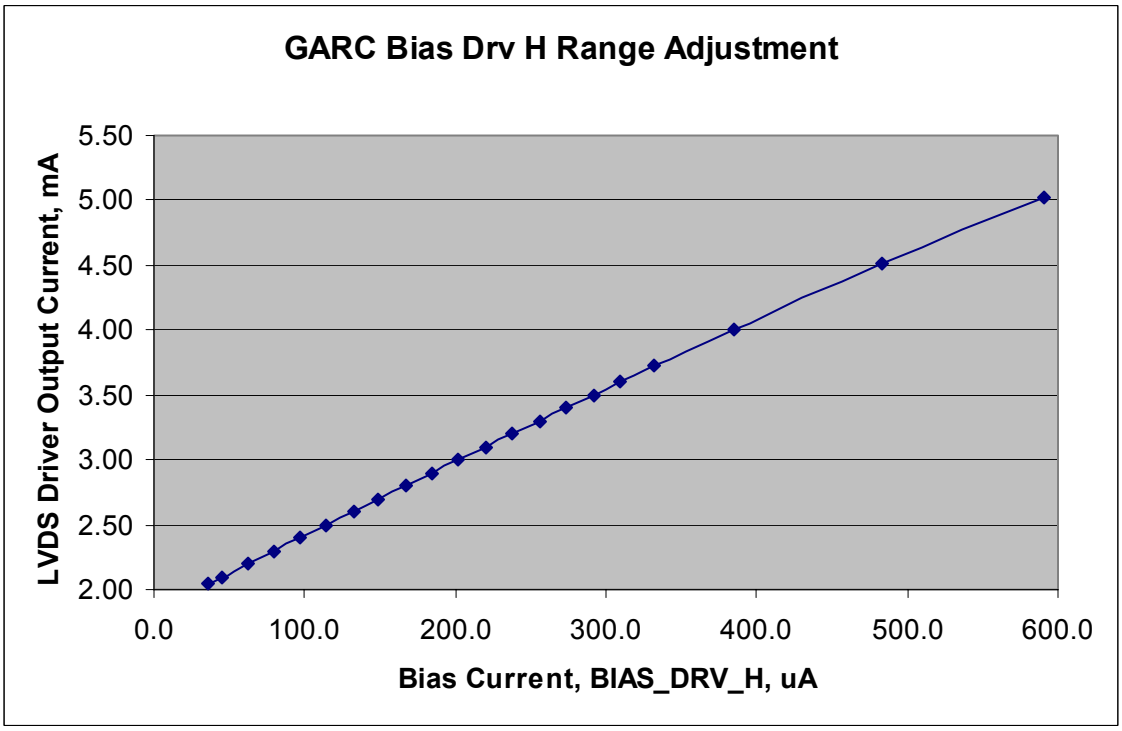
Bias	Test Board Res	V(Resistor)	Resistor Value	Calculated Bias Current
Bias_Drv_H	R15	1.135	7.81 kΩ	145.3 μA
Bias_Drv_L	R13	1.568	16.37 kΩ	95.8 μA
Rcvr_Bias	R16	2.259	84.90 kΩ	26.6 μA
WOR_Bias	R19	1.603	7.88 kΩ	203.3 μA
LVDS_Preset_Adj	R20	1.896	5.81 kΩ	326.3 μA

In this biasing configuration, at 3.3V, the LVDS driver current in the termination resistor on the NSDATA_A driver is 2.99 mA. The LVDS preset is measured at 1.378V / 1.079 V.

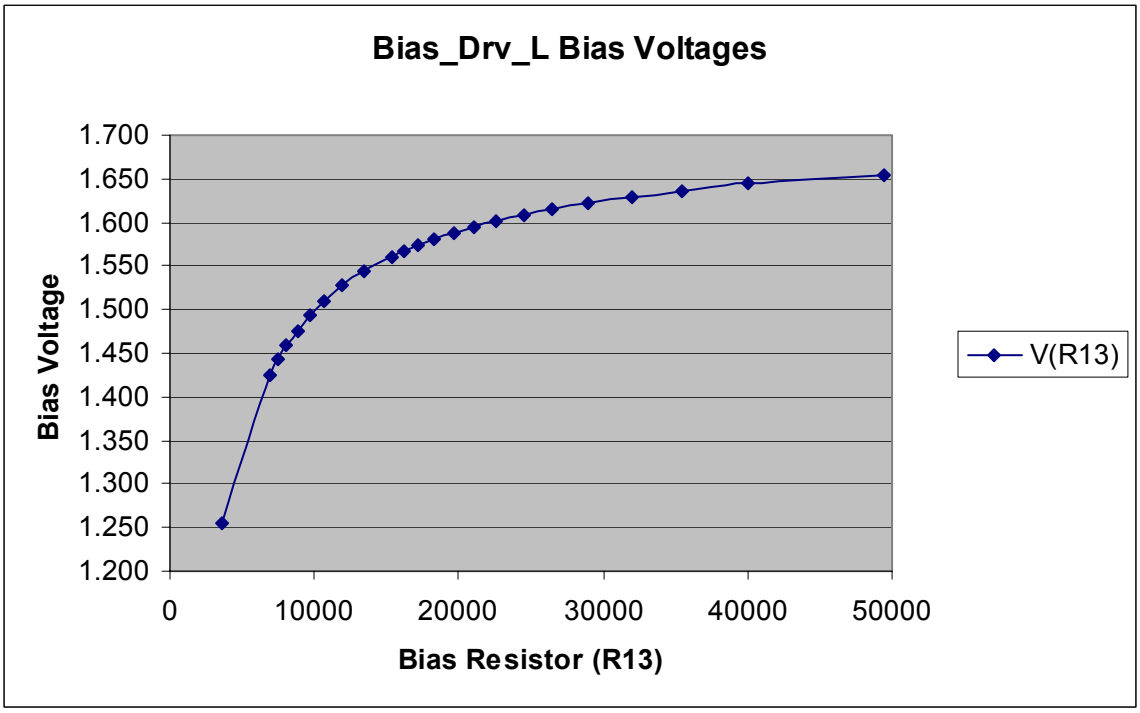
GARC Voltage	GARC Current (mA)	GARC Mode (decimal)	VETO A Drivers	VETO B Drivers
2.993	104.88	768	On	On
2.993	76.29	256	On	Off
2.993	75.40	512	Off	On
2.993	41.54	0	Off	Off
3.310	125.31	768	On	On
3.310	90.92	256	On	Off
3.310	89.85	512	Off	On
3.310	49.34	0	Off	Off
3.609	144.83	768	On	On
3.609	104.98	256	On	Off
3.609	103.80	512	Off	On
3.609	56.83	0	Off	Off

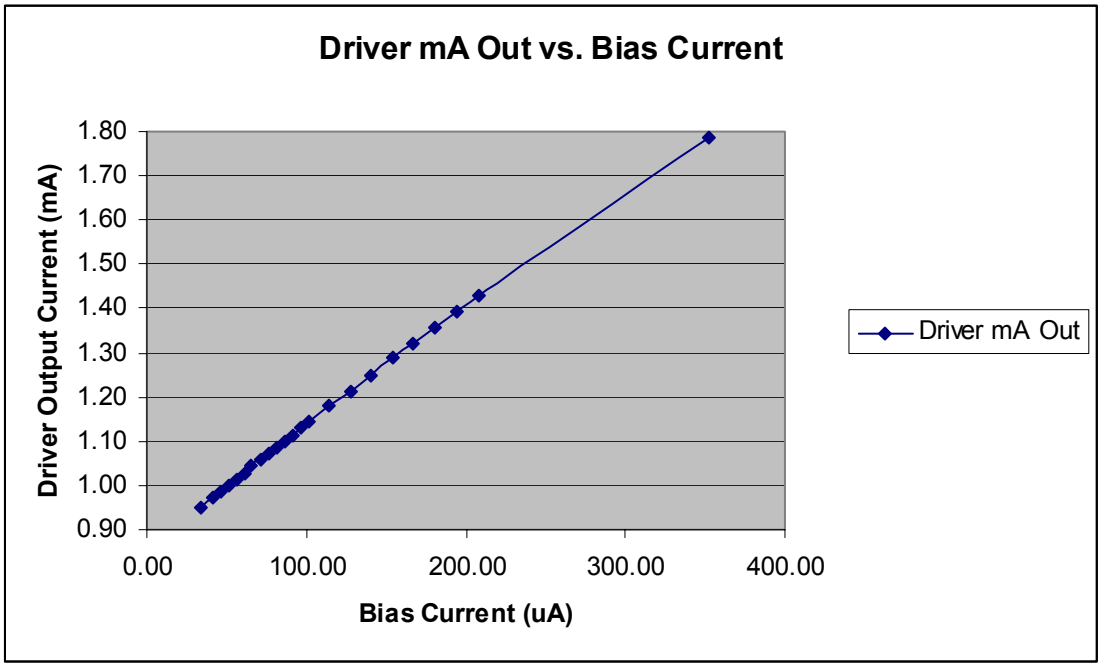
A preliminary attempt to explore the range of biasing parameters was made. The following data represents the BIAS_DRV_H adjustment, which controls the driver currents for signals at the ACD interface.



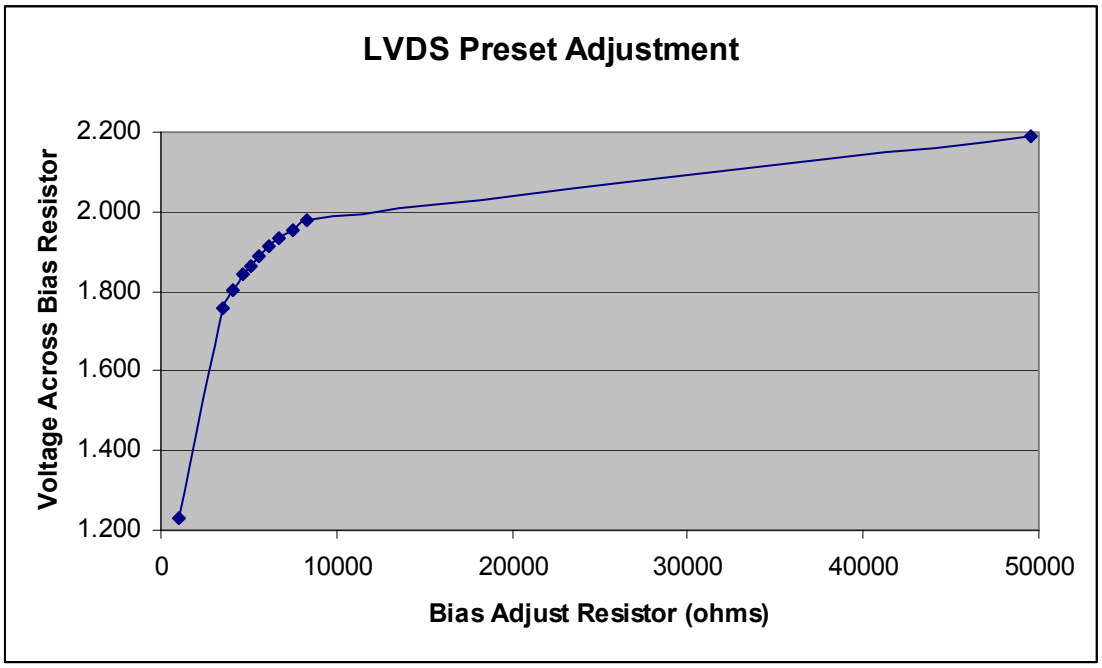


The following data represents the BIAS_DRV_L adjustment, which controls the LLVDS driver currents from the GARC to the GAFE.

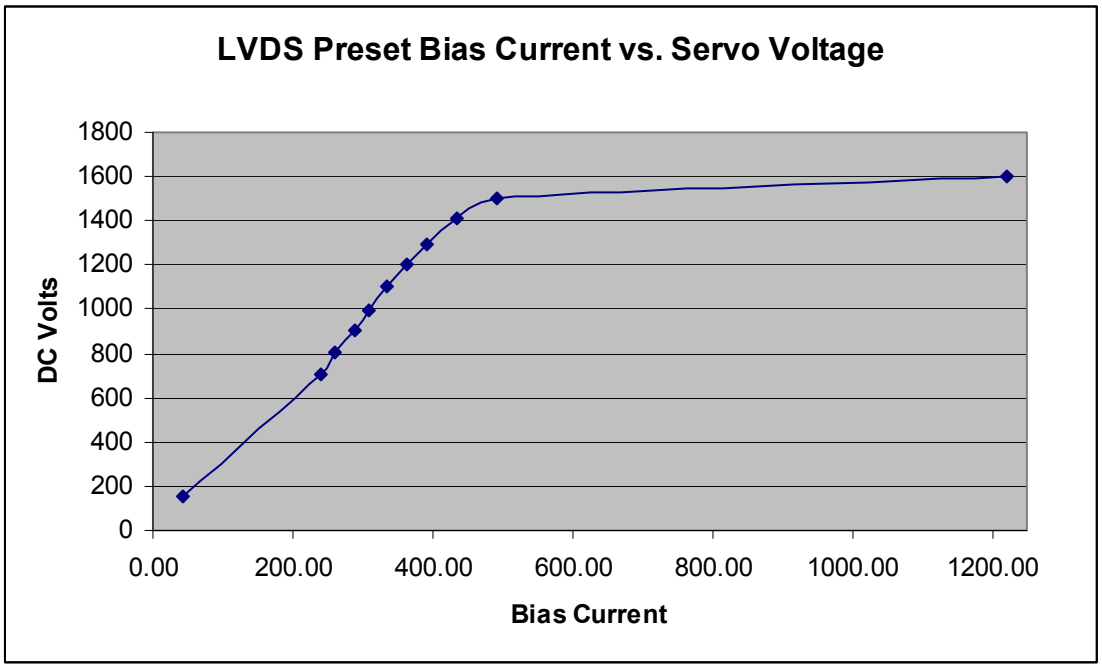




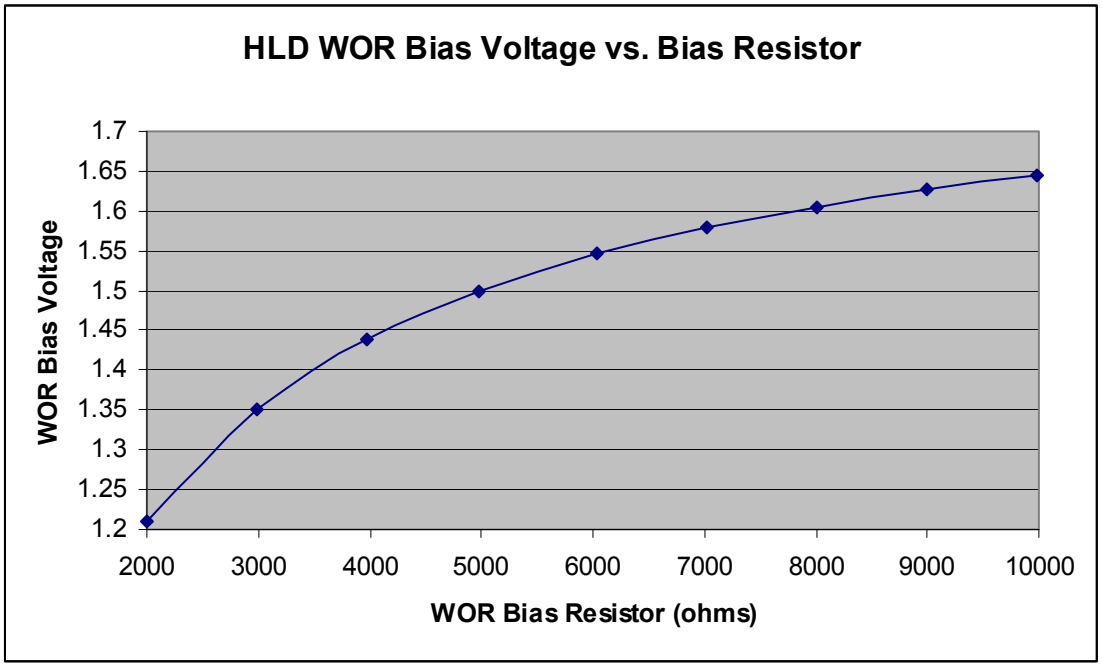
The following data represents the LVDS_PRESET adjustment which controls the DC bias level of the LVDS drivers.

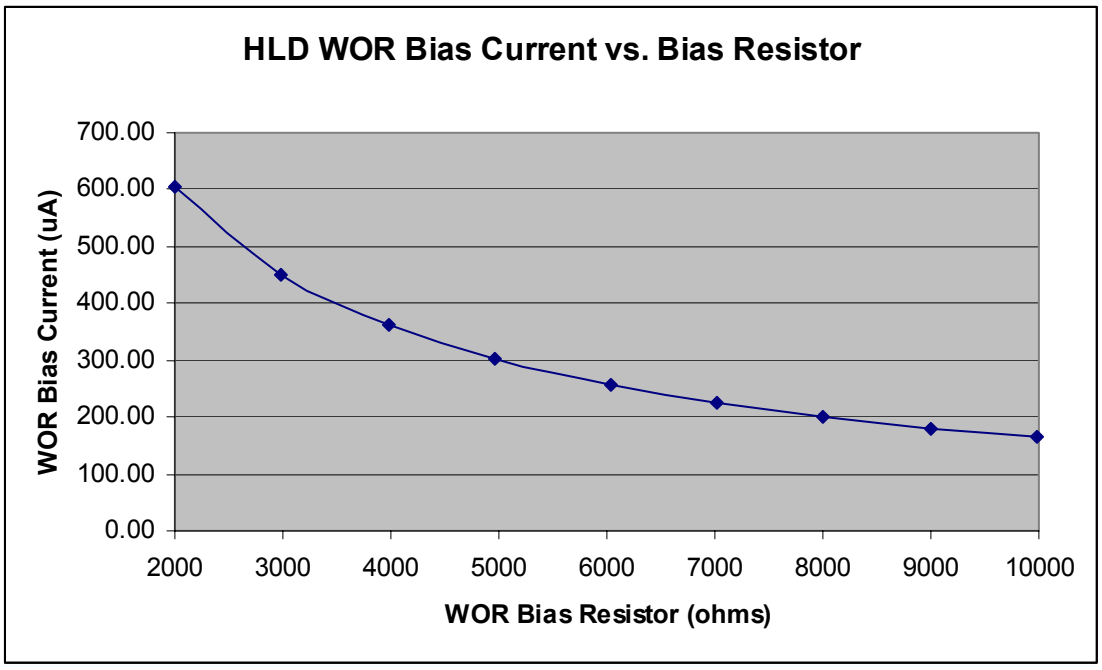


The servo voltage plotted represents the larger of the two voltages across the 100 Ω termination resistor on the NSDATA_A driver. During this test, the LVDS driver current was approximately 3 mA for this signal.



The following data represents the HLD WOR BIAS adjustment.





The following data was recorded for the BIAS_DRV_H adjustment:

R15 (ohms)	V(R15)	I(Bias_Drv_H), uA	mV(R30)	Driver mA Out
49500	1.758	35.5	204	2.04
38200	1.747	45.7	210	2.10
27600	1.728	62.6	220	2.20
21300	1.708	80.2	230	2.30
17320	1.689	97.5	240	2.40
14600	1.671	114.5	250	2.50
12460	1.652	132.6	260	2.60
10980	1.635	148.9	270	2.70
9660	1.617	167.4	280	2.80
8680	1.599	184.2	290	2.90
7850	1.582	201.5	300	3.00
7110	1.564	220.0	310	3.10
6510	1.547	237.6	320	3.20
5970	1.529	256.1	330	3.30
5540	1.513	273.1	340	3.40
5130	1.496	291.6	350	3.50
4780	1.478	309.2	360	3.60
4400	1.459	331.6	372	3.72
3660	1.410	385.2	401	4.01
2740	1.325	483.6	451	4.51
2090	1.235	590.9	502	5.02

The following data was recorded for the BIAS_DRV_L adjustment:

R13 (ohms)	V(R13)	I(Bias_Drv_L), uA	mV(R83)	Driver mA Out
49500	1.654	33.41	665	0.95
40000	1.644	41.10	680	0.97
35400	1.636	46.21	690	0.99
32000	1.630	50.94	700	1.00
29000	1.623	55.97	710	1.01
26500	1.616	60.98	720	1.03
24500	1.609	65.67	730	1.04
22600	1.602	70.88	740	1.06
21000	1.595	75.95	750	1.07
19630	1.588	80.90	760	1.09
18310	1.581	86.35	770	1.10
17230	1.574	91.35	780	1.11
16240	1.567	96.49	790	1.13
15340	1.560	101.69	800	1.14
13450	1.543	114.72	825	1.18
11970	1.527	127.57	850	1.21
10730	1.510	140.73	875	1.25
9690	1.493	154.08	901	1.29
8840	1.476	166.97	925	1.32
8090	1.459	180.35	950	1.36
7440	1.442	193.82	976	1.39
6860	1.425	207.73	1001	1.43
3560	1.256	352.81	1251	1.79

The following data was recorded for the LVDS_PRESET adjustment:

LVDS Preset Adjustment			
R20	**V(R20)**	**Bias Current (uA)**	**V(J2-37), mV**
49500	2.190	44.24	157
8270	1.977	239.06	703
7490	1.956	261.15	801
6720	1.934	287.80	902
6200	1.913	308.55	998
5620	1.888	335.94	1106
5130	1.864	363.35	1207
4710	1.841	390.87	1294
4140	1.803	435.51	1409
3560	1.756	493.26	1501
1008	1.230	1220.24	1604

The following data was recorded for the HLD_WOR_BIAS adjustment:

R19 is the WOR Bias Adjustment		
Schematic says 260 uA is the desired bias.		
R19 (ohms)	**V(R19)**	**I(R19) uA**
9990	1.644	164.56
9000	1.626	180.67
8000	1.605	200.63
7020	1.579	224.93
6030	1.546	256.38
4970	1.499	301.61
3980	1.439	361.56
2990	1.351	451.84
2000	1.209	604.50

Appendix 2: GARC V1 Delay and Timing Measurements

(from 9/19/2002 RGB write-up)

Some quick look delay and timing measurements on GARC1.

Delay from CLK_AP to:	GARC1 #6 (nsec)	miniGARC1 #2 (nsec)
NVETO_00AP	18.4	
NSDATA_AP	19.6	31/37 (-/+ edge)
DAC_CLK	18.4	24.4
DAC_DATA	20.9	26.4
NADC_CS	20.3	26.8
HV_ENABLE_1	21.0	27.8
HV_ENABLE_2	23.4	
HITMAP_TEST	28.5	
TRIG_TEST	26.4	

Delay, ck to GAFE_RST: 40.0 nsec. (GARC reset command)
(ck to GAFE_RST deassert: 21.4)

Delay, ck to GAFE_RST deassert: 21.5 nsec. (Sig from AEM)
ck to GAFE_RST assert: 35.0 nsec.

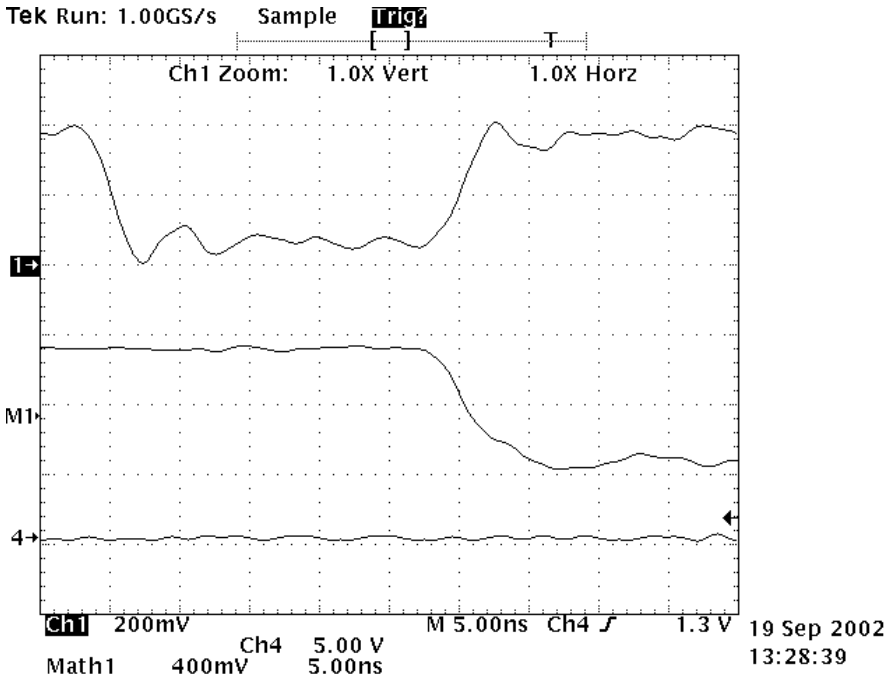
Width of GAFE_RST: 82.6 nsec.

On GAFE2, delay ck to state bit output: 26 nsec.

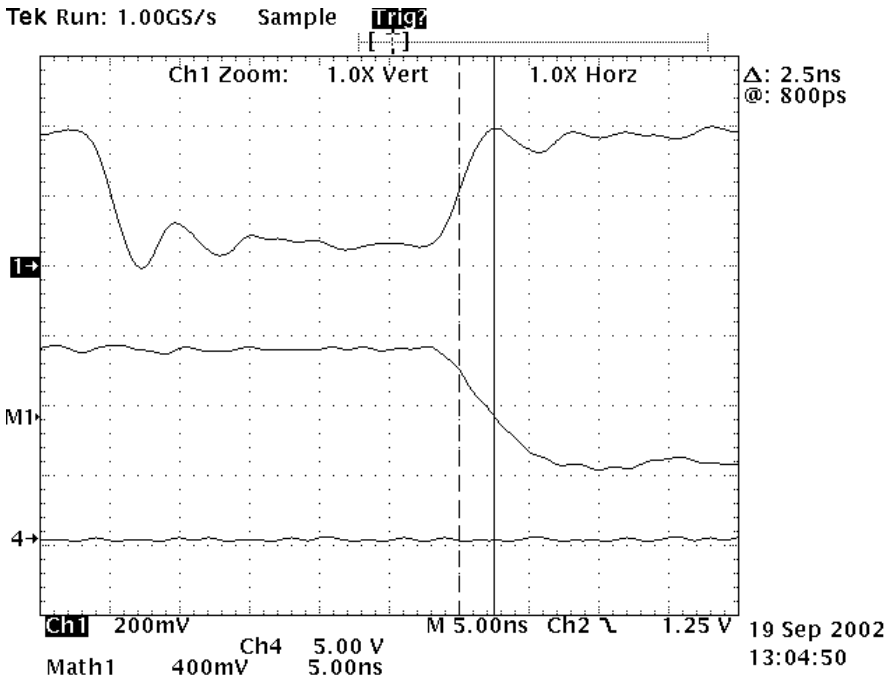
Added delay line between AEM simulator and GARC on the NSCMD only. Twisted #30 wirewrap wire. This was to determine when does the command data need to be at the GARC for functionality. Pictures show that the command must be at or before the positive clock edge. There is a delay setting where the GARC does not work. Since the AEM will shift the command out on the negative clock edge, the command transitions will arrive at the GARC well away from the problem point.

The GARC shifts return data (NSDATA) out on the positive clock edge. Delay in the GARC from clock to NSDATA is around 20 nsec.

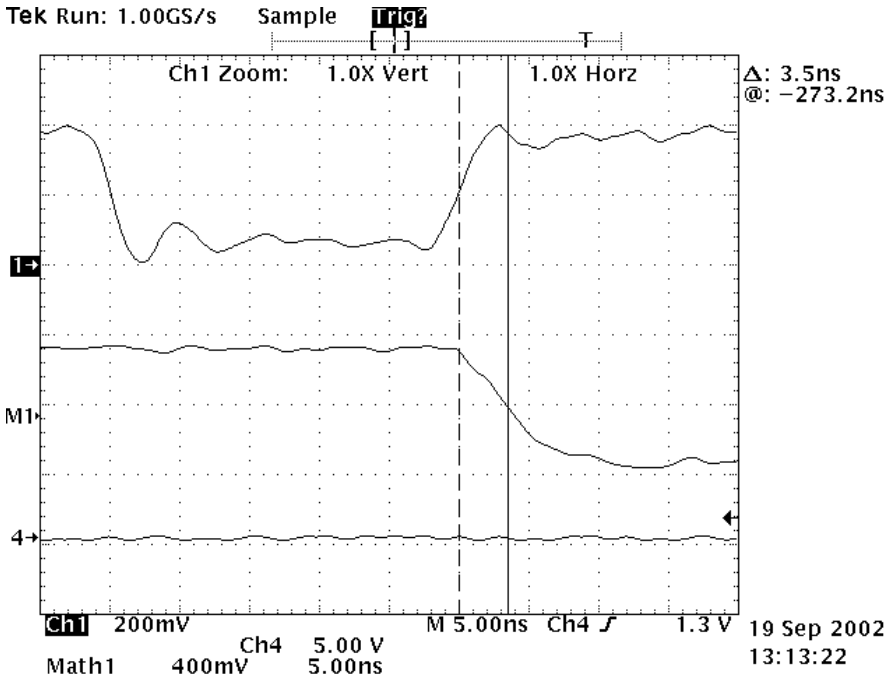
Picture shows CLK_AP and NSCMD (differential) with 4.65 meters of extra cable on NSCMD. Cable adds 25 nsec. GARC sees logic zero on this positive edge.



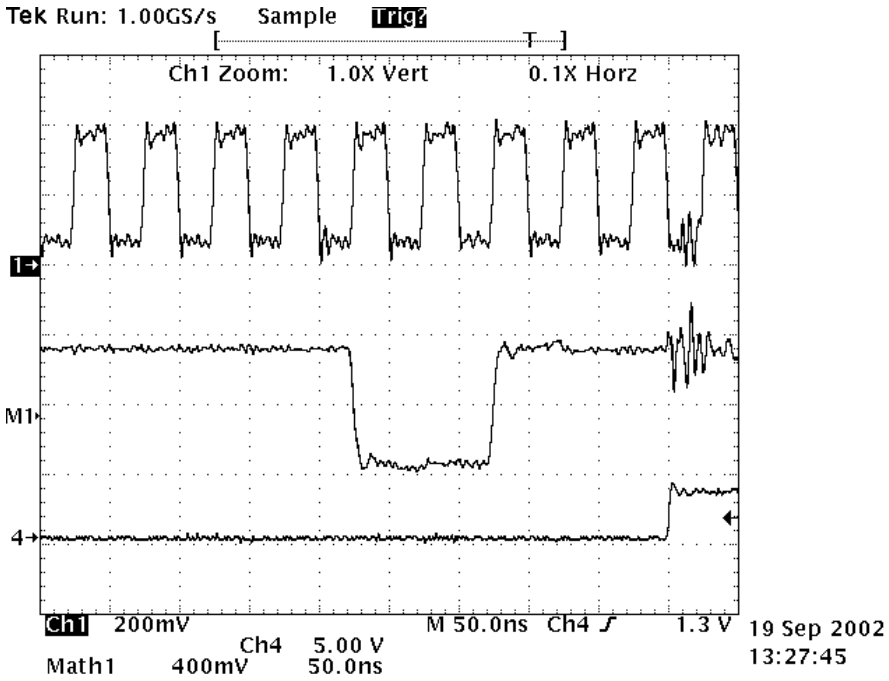
Picture shows CLK_AP and NSCMD (differential) with 4.90 meters of extra cable on NSCMD. Cable adds 27 nsec. NSCMD is undefined to GARC, no functionality.

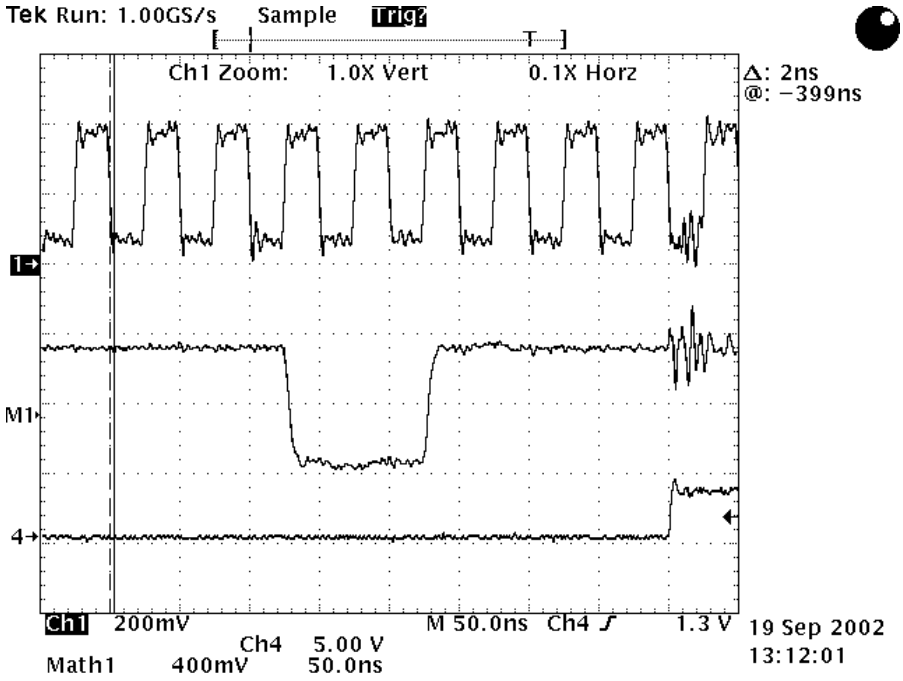


Picture shows CLK_AP and NSCMD (differential) with 5.15 meters of extra cable on NSCMD. Cable adds almost 29 nsec. GARC sees logic one on this positive edge. Signal is delayed enough for GARC to miss data, catch it on the next edge.



The following two pictures are at 50 nsec/div for the 4.65 and 5.15 meter cases above. They show TRIG_TEST on channel 4. The 5.15 m case shows the bit slip.




Tek Run: 1.00GS/s Sample Trig?
Ch1 Zoom: 1.0X Vert 0.1X Horz
Δ: 2ns
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1→
M1
4→
Ch1 200mV
M 50.0ns Ch4 ƒ 1.3 V
Ch4 5.00 V
Math1 400mV 50.0ns
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